

# Micro-Policies

A Framework for Verified, Hardware-Assisted  
Security Monitors

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# Current collaborators on this project

- **Formal verification side**

- Arthur Azevedo de Amorim (UPenn & INRIA Paris)
- Maxime Dénès (UPenn)
- Nick Giannarakis (INRIA Paris & NTU Athens)
- Cătălin Hrițcu (INRIA Paris)
- Benjamin Pierce (UPenn)
- Antal Spector-Zabusky (UPenn)
- Andrew Tolmach (Portland State)

- **Architecture side**

- André DeHon, Udit Dhawan, Nikos Vasilakis, ... (UPenn)

# Computer systems are insecure



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- Today's CPUs are mindless bureaucrats
  - “write past the end of this buffer” *... yes boss!*
  - “jump to this untrusted integer” *... right boss!*
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- Software bears most of the burden for security
  - pervasive security enforcement impractical
  - security-performance tradeoff
  - just write secure code ... all of it!
- Consequence: vulnerabilities in every system
  - violations of known safety and security policies



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  - tags and rules **defined by software** (miss handler; verified)
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  - tags efficiently propagated on each instruction
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- low overhead: <10% runtime, <50% energy, <12% power

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- monitor self-protection
- dynamic sealing
  - compartmentalization
  - memory safety
- control-flow integrity (CFI)
- hardware types (instr/ptr/...)
  - taint tracking
- ...

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recent  
draft

Verified  
(in Coq)



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Evaluated  
(simulations)

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## **memory safety**

- control-flow integrity (CFI)
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recent  
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# Memory safety

- Prevent
  - **spatial violations**: reading/writing out of bounds
  - **temporal violations**: use after free, invalid free



# Memory safety

- Prevent
  - **spatial violations**: reading/writing out of bounds
  - **temporal violations**: use after free, invalid free
- Pointers become **unforgeable capabilities** 
  - can only obtain a valid pointer to a memory region
    - by allocating that region or
      - by copying/offsetting an existing pointer to that region

# Memory safety micro-policy

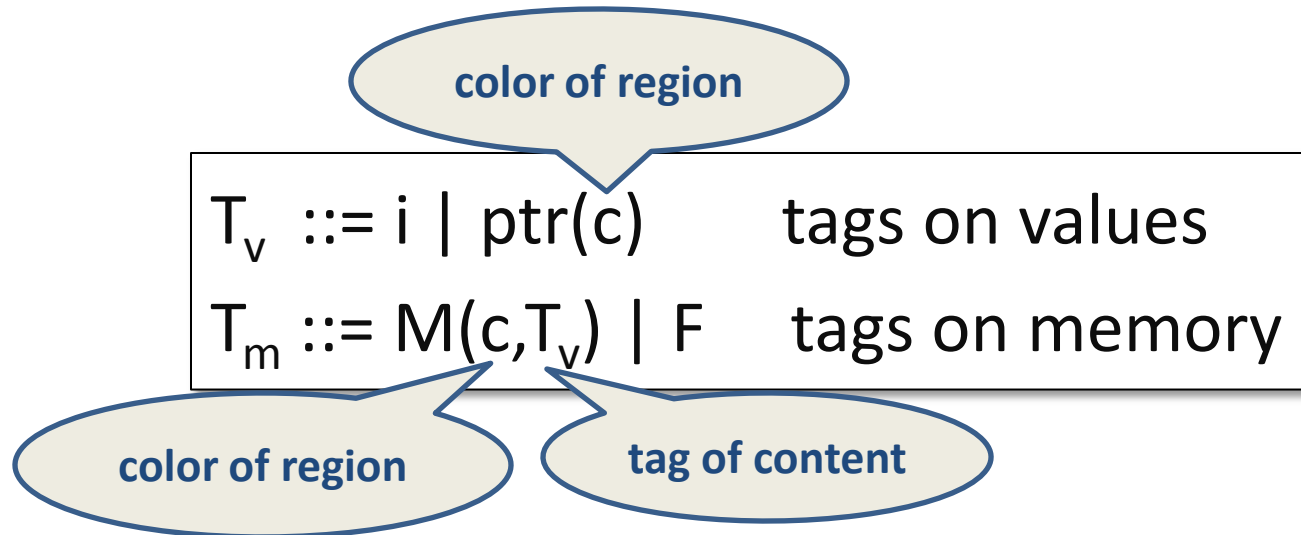
$T_v ::= i \mid \text{ptr}(c)$	tags on values
$T_m ::= M(c, T_v) \mid F$	tags on memory

# Memory safety micro-policy

color of region

$T_v ::= i \mid \text{ptr}(c)$	tags on values
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# Memory safety micro-policy



# Memory safety micro-policy

$p \leftarrow \text{malloc } k$

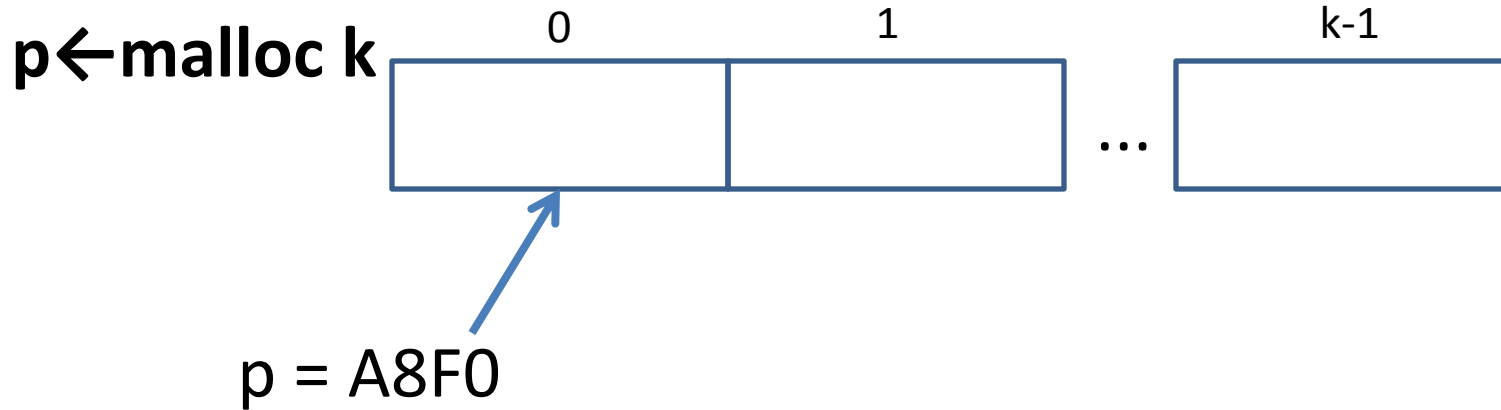
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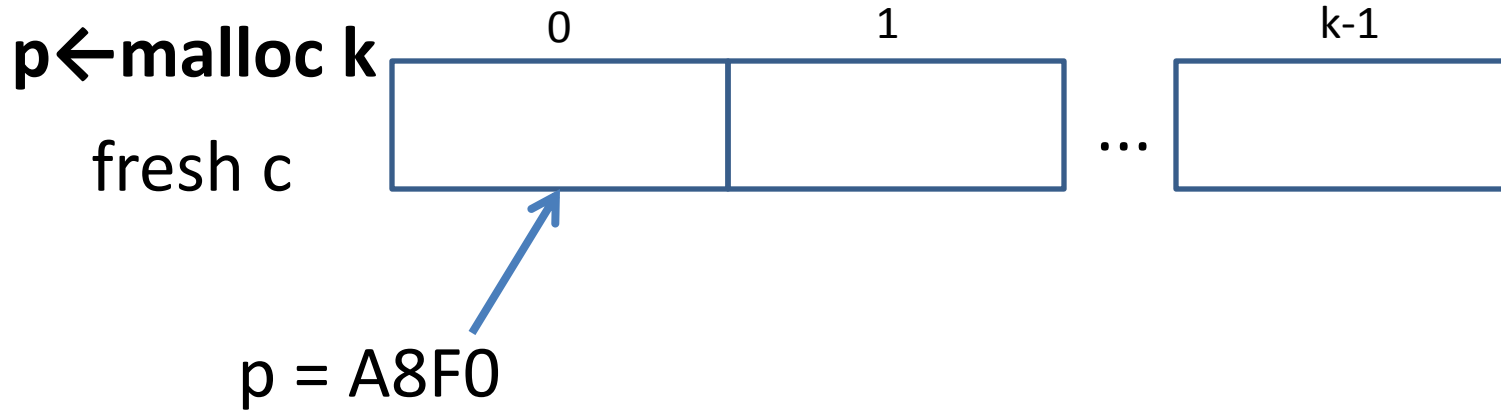
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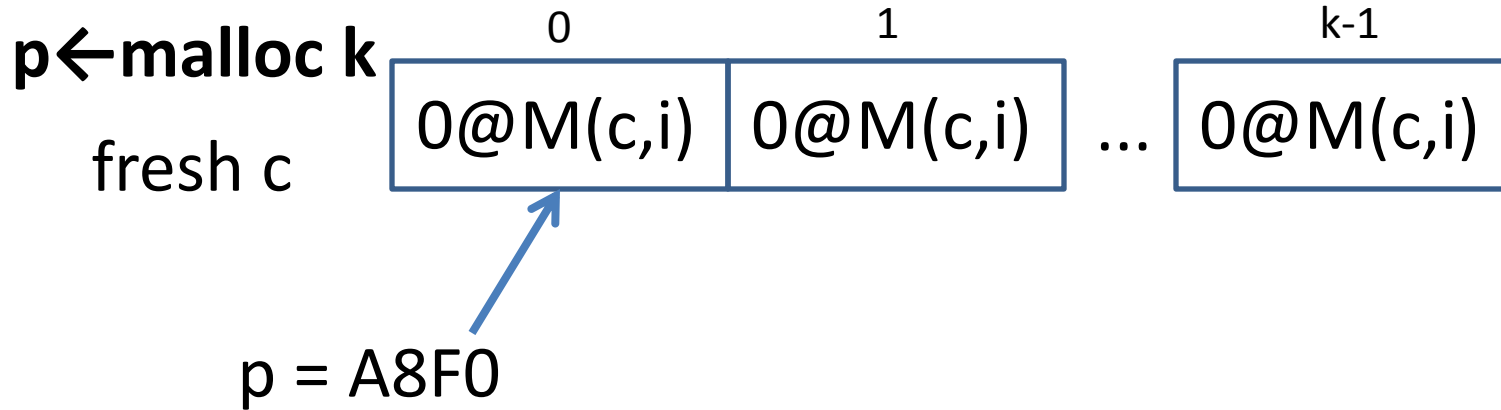
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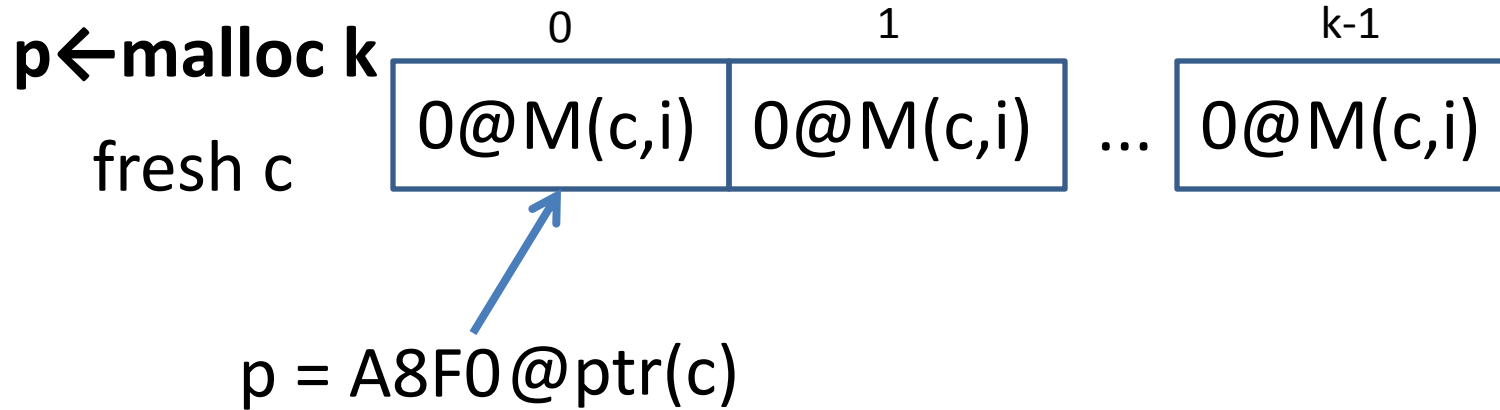


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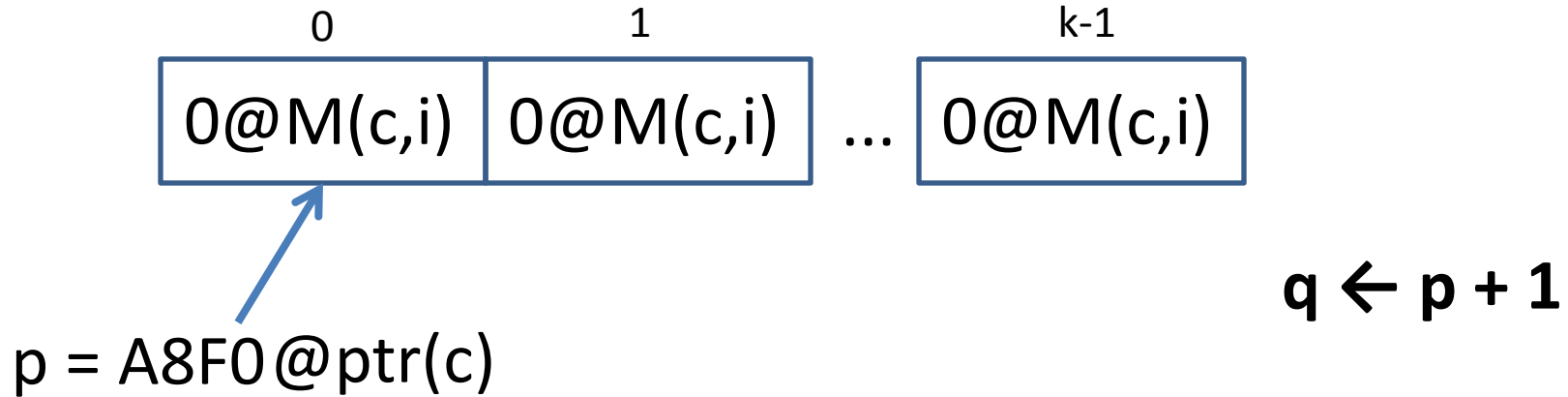
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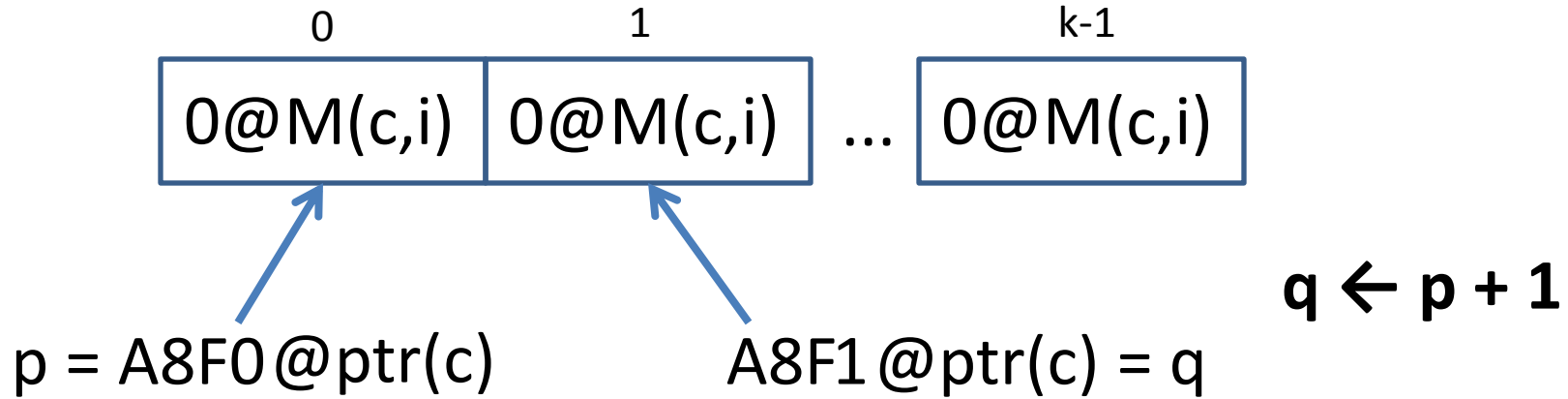
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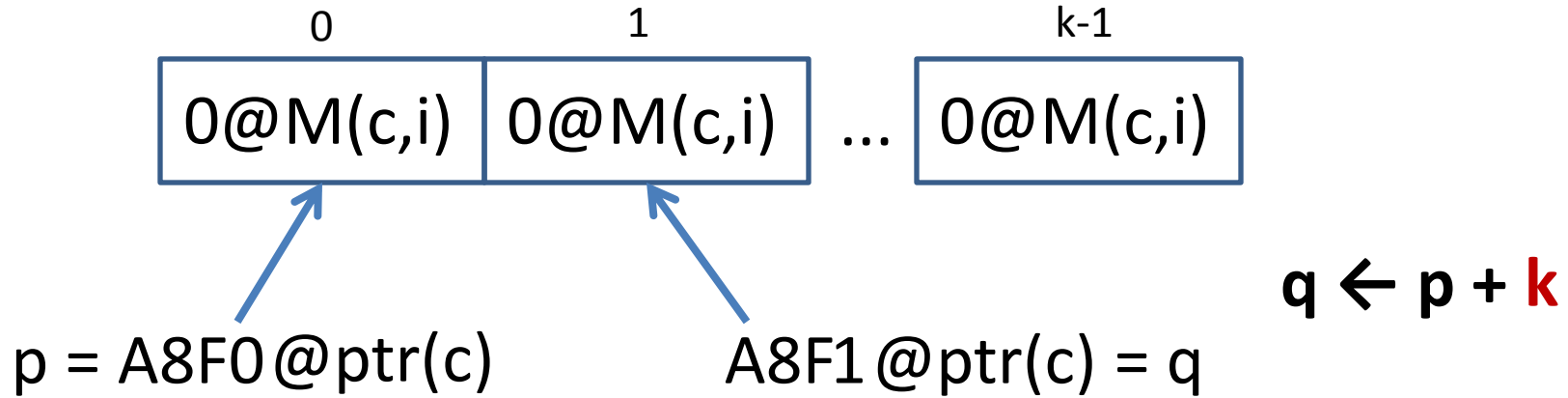
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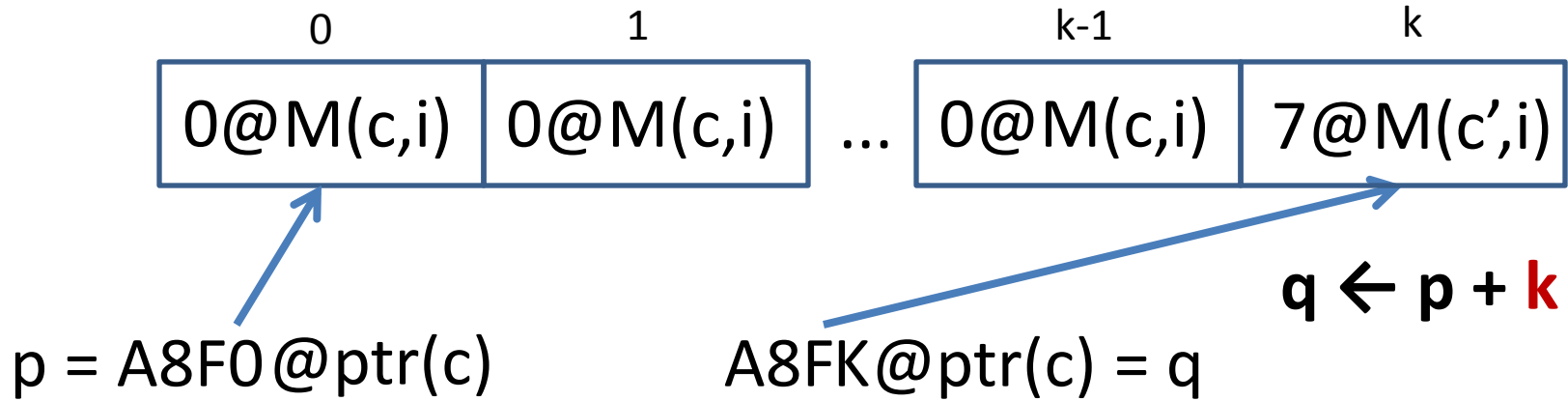
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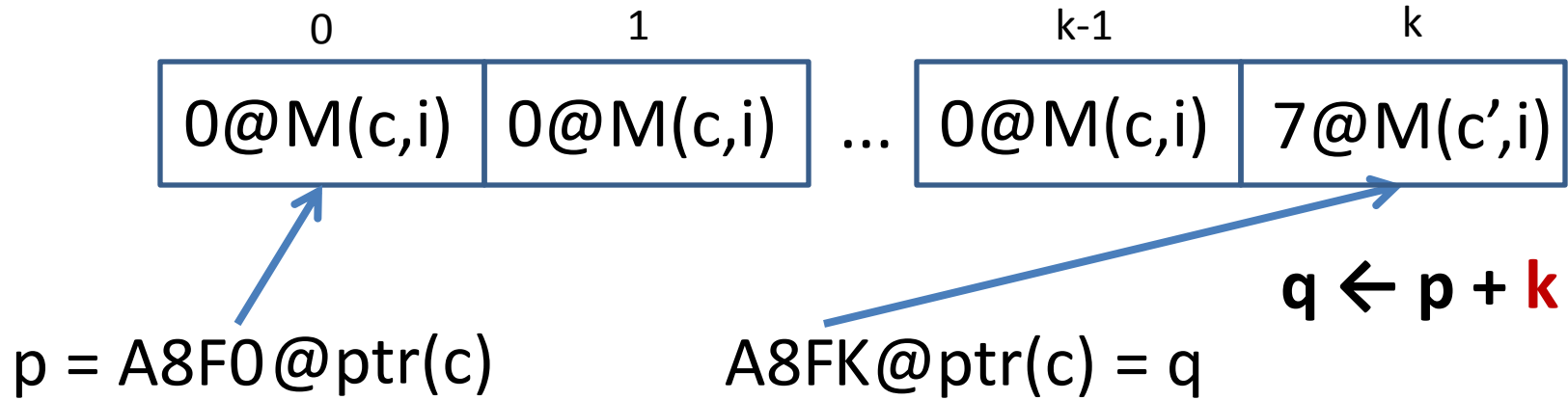
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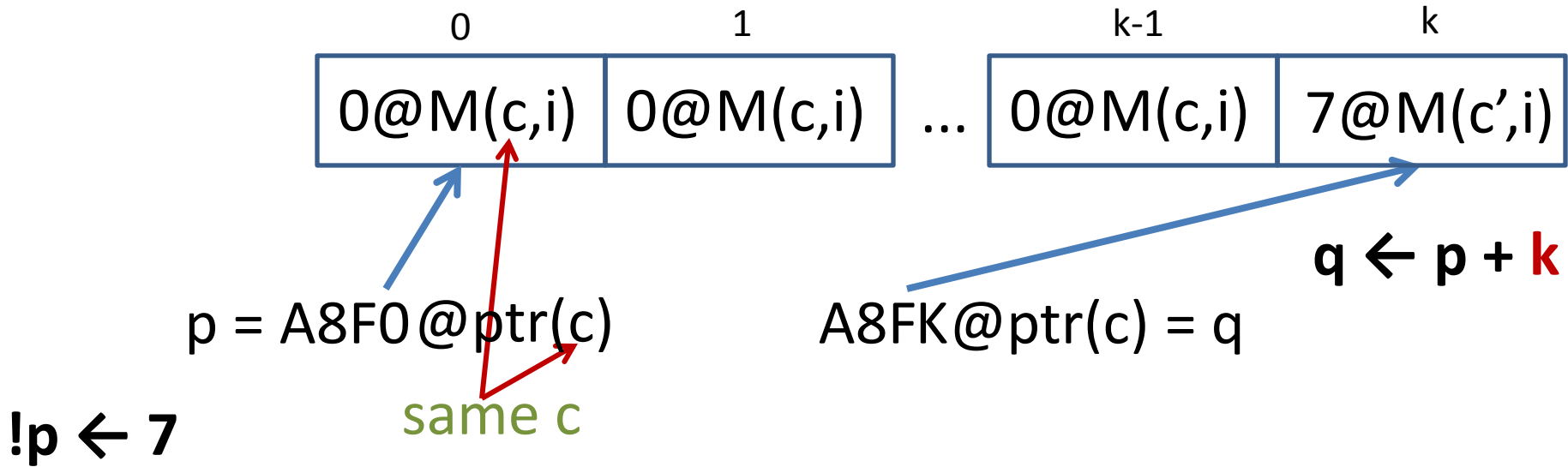
# Memory safety micro-policy



**$!p \leftarrow 7$**

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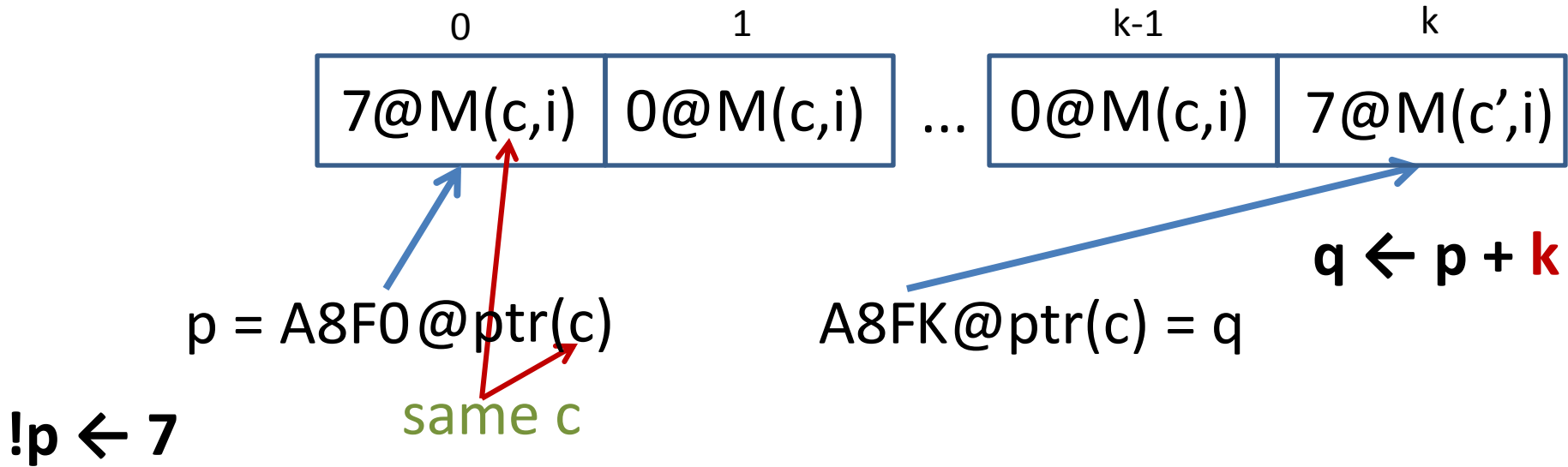
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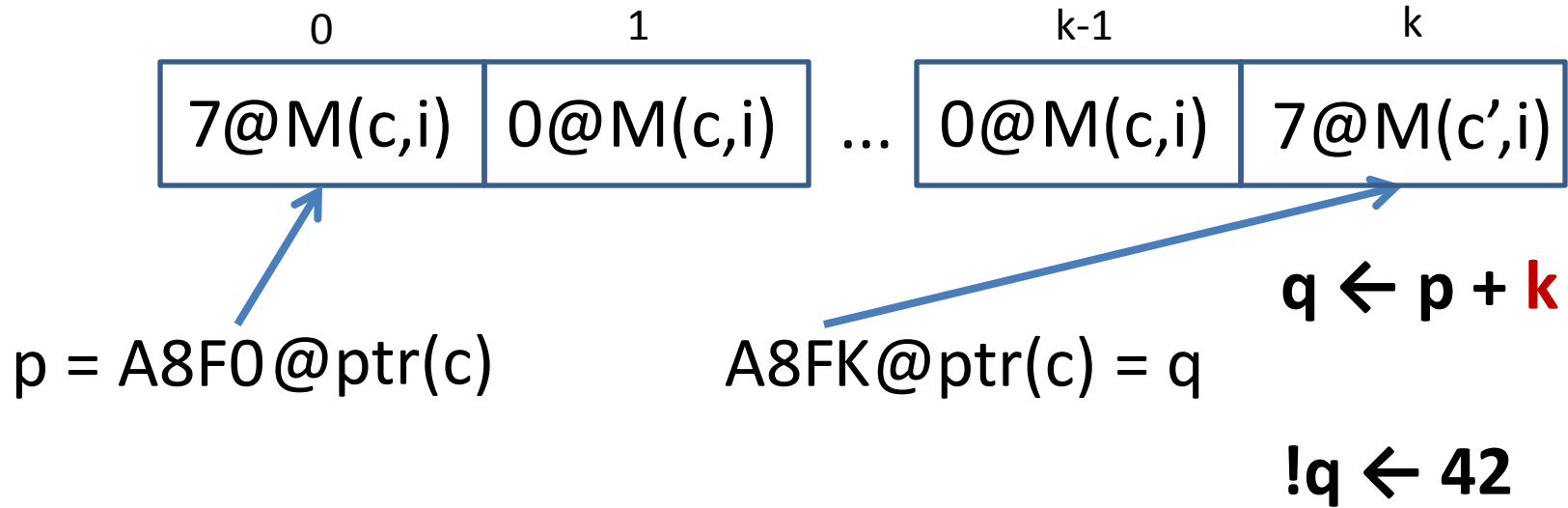


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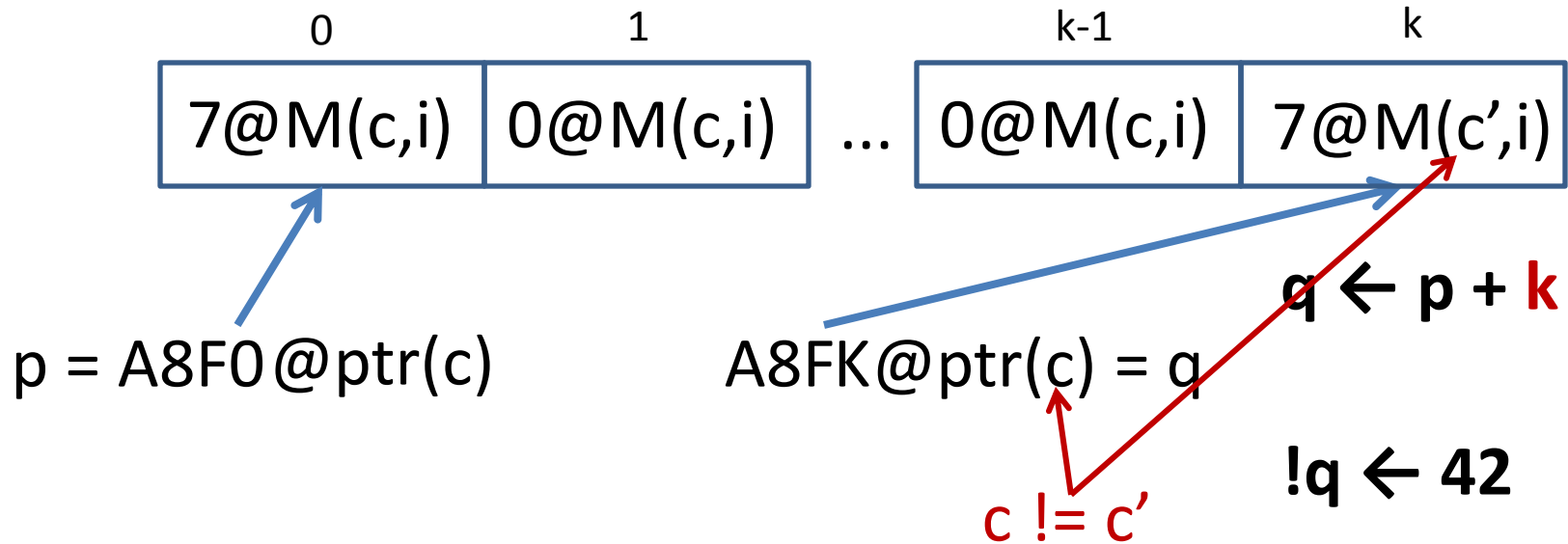
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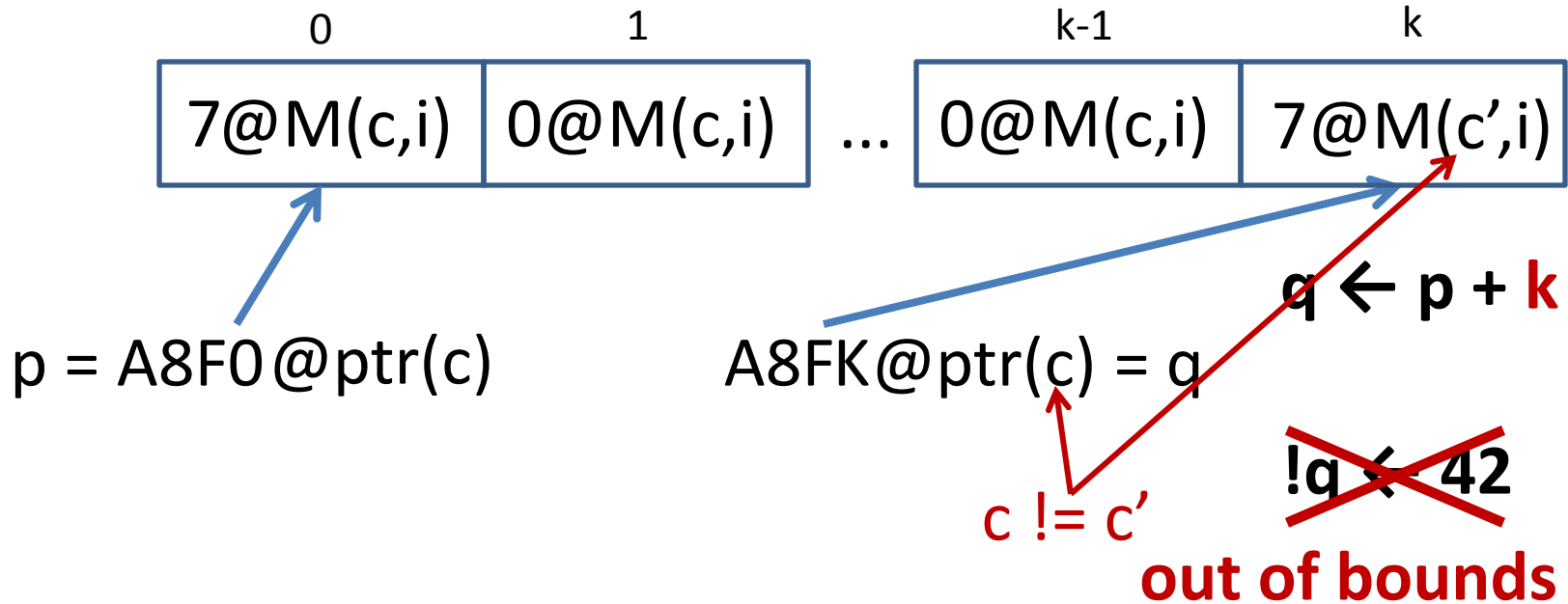
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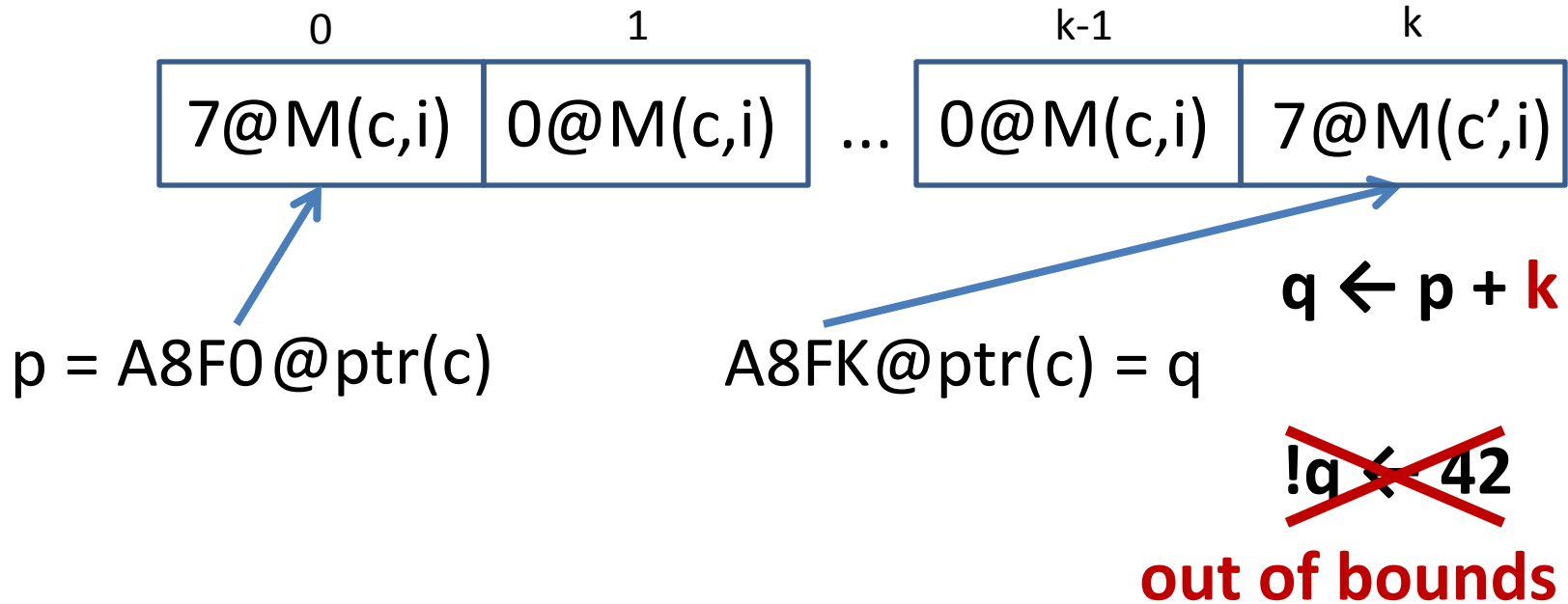
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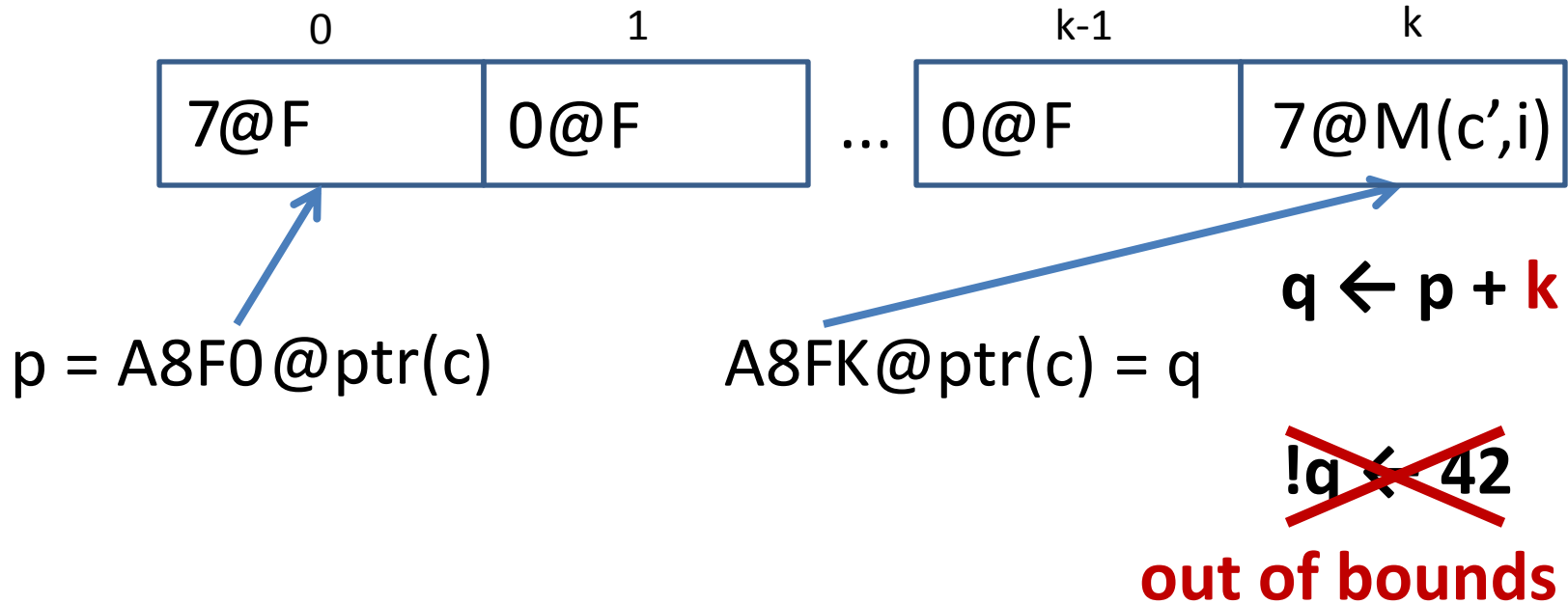
# Memory safety micro-policy



**free p**

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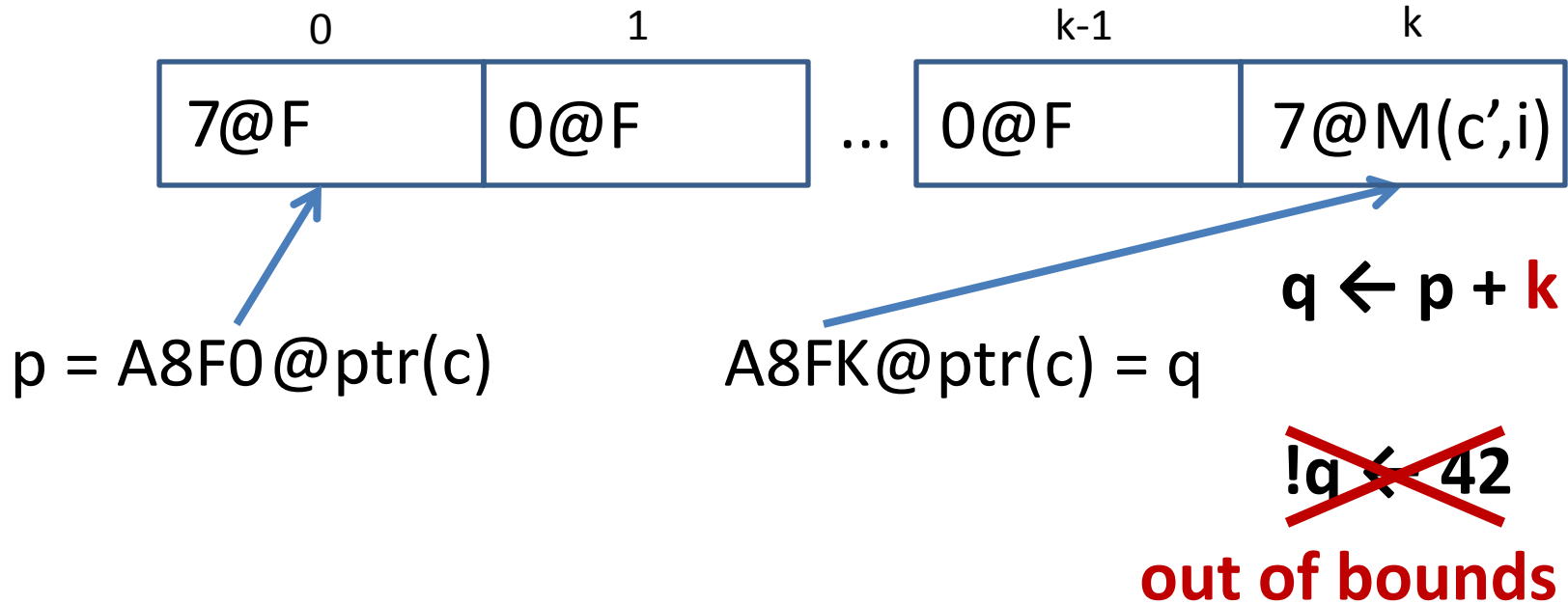
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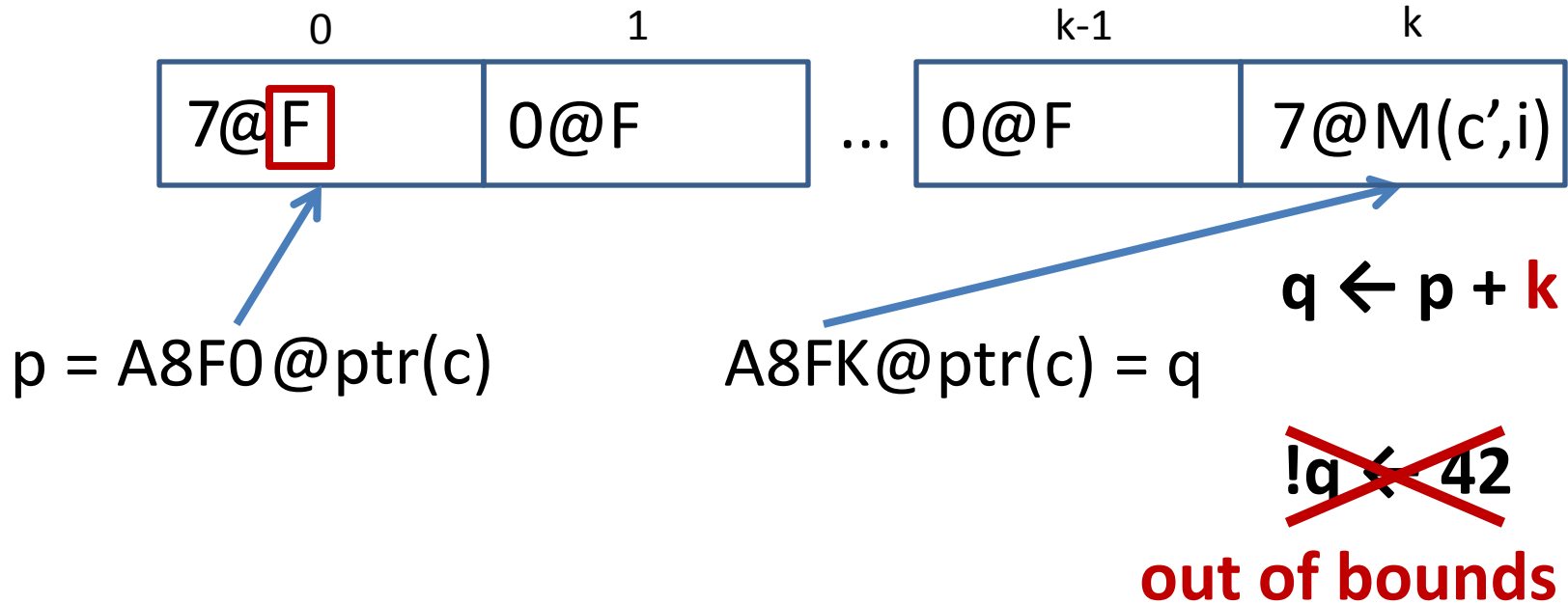


free p

$x \leftarrow !p$

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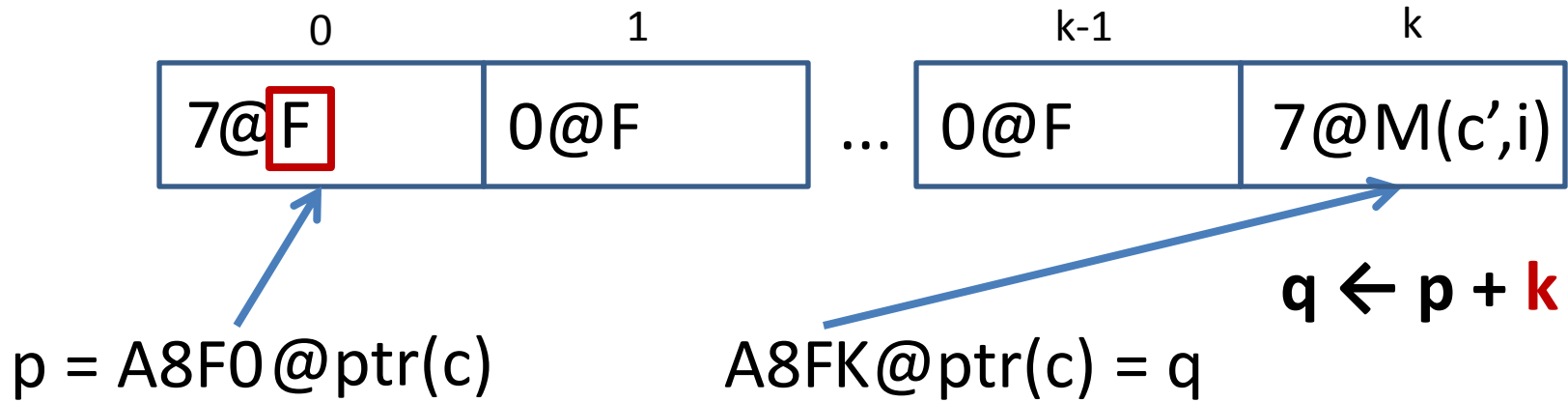
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**out of bounds**

free p

~~$x \leftarrow !p$~~

**use after free**

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## 1. Sets of tags

$$T_v ::= i \mid \text{ptr}(c)$$
$$T_m ::= M(c, T_v) \mid F$$
$$T_{pc} ::= T_v$$

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## 2. Transfer function

Record IVec := { op:opcode ;  $t_{pc}:T_{pc}$  ;  $t_i:T_m$  ; ts: ... }

Record OVec (op:opcode) := {  $t_{rpc} : T_{pc}$  ;  $t_r : \dots$  }

transfer : (iv:IVec) -> option (OVec (op iv))

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match iv with

| {op=Load;  $t_{pc}=\text{ptr}(c_{pc})$ ;  $t_i=M(c_{pc}, i)$ ; ts=[ptr(c); M(c,  $T_v$ )]}

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=> { $t_{rpc}=\text{ptr}(c_{pc})$ ;  $t_r=T_v$ }

| {op=Store;  $t_{pc}=\text{ptr}(c_{pc})$ ;  $t_i=M(c_{pc}, i)$ ; ts=[ptr(c);  $T_v$ ; M(c,  $T_v'$ )]}

=> { $t_{rpc}=\text{ptr}(c_{pc})$ ;  $t_r=M(c, T_v)$ }

...

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## 3. Monitor services

Record service := { addr : word; sem : state -> option state; ... }

Definition mem\_safety\_services : list service :=

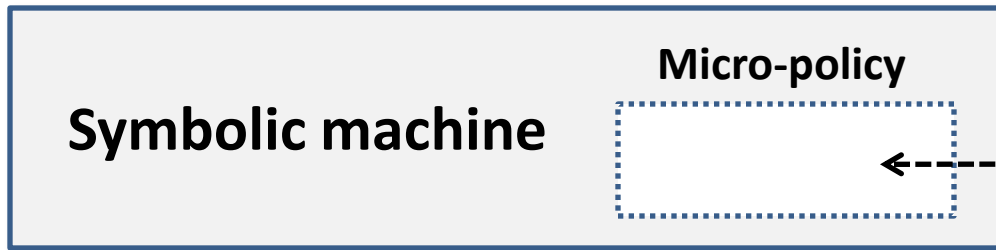
[malloc; free; size; base; eq].

**memory safety  
micro-policy**

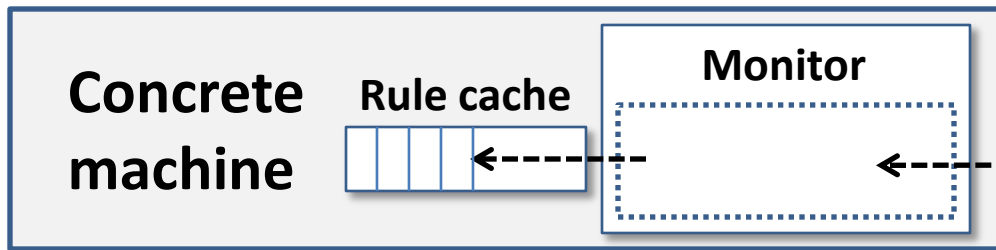








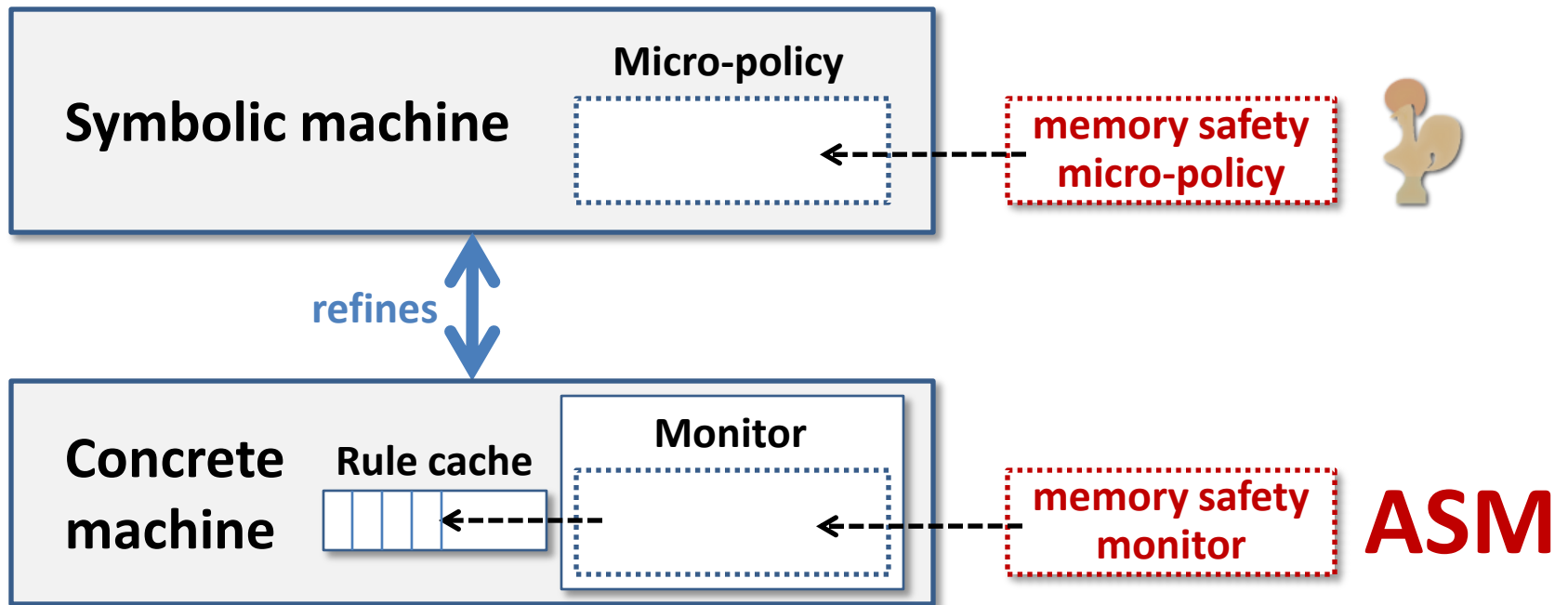
memory safety  
micro-policy



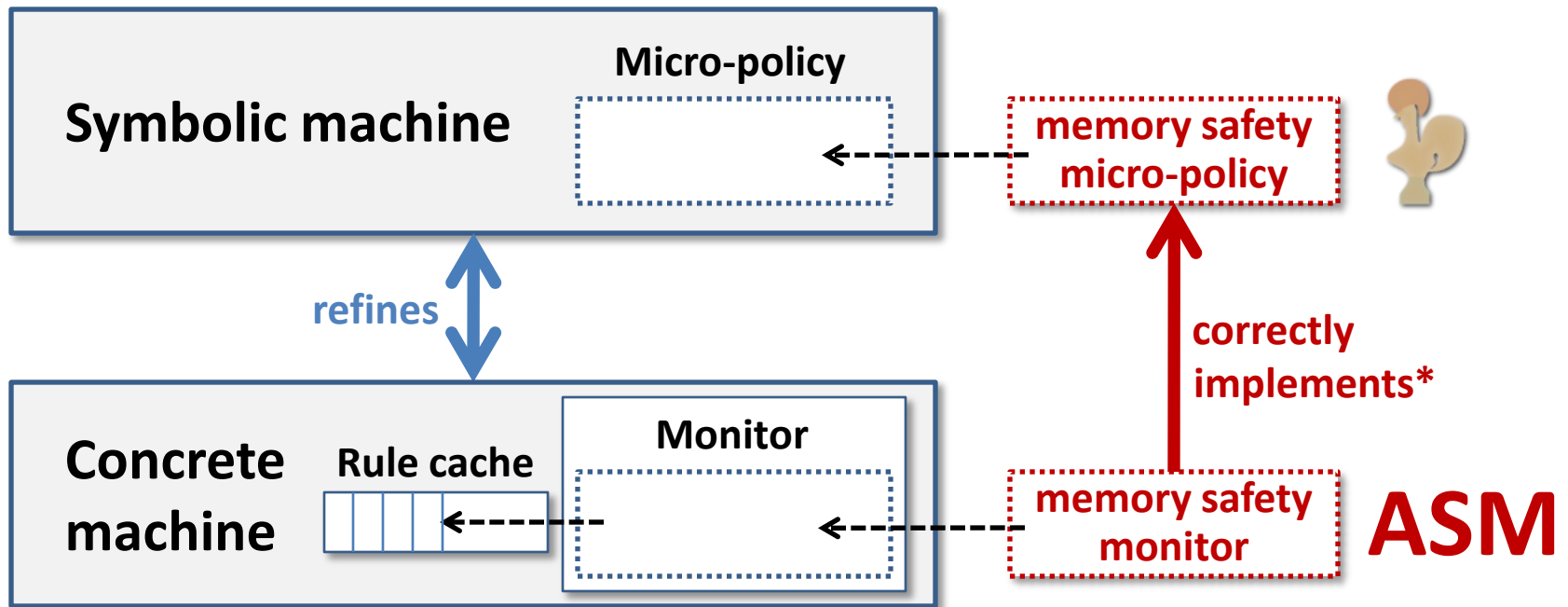
memory safety  
monitor

**ASM**

# Verification

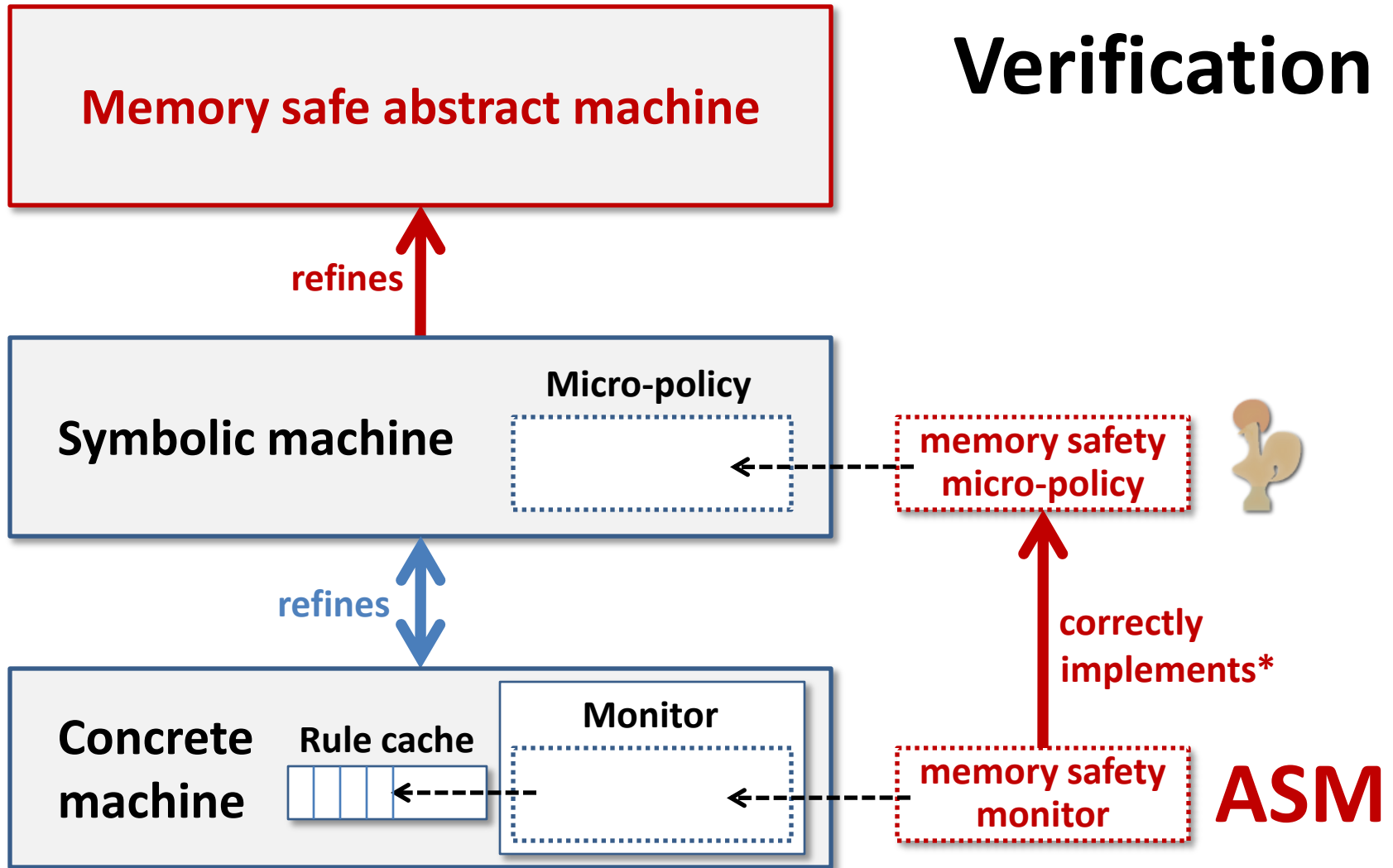


# Verification



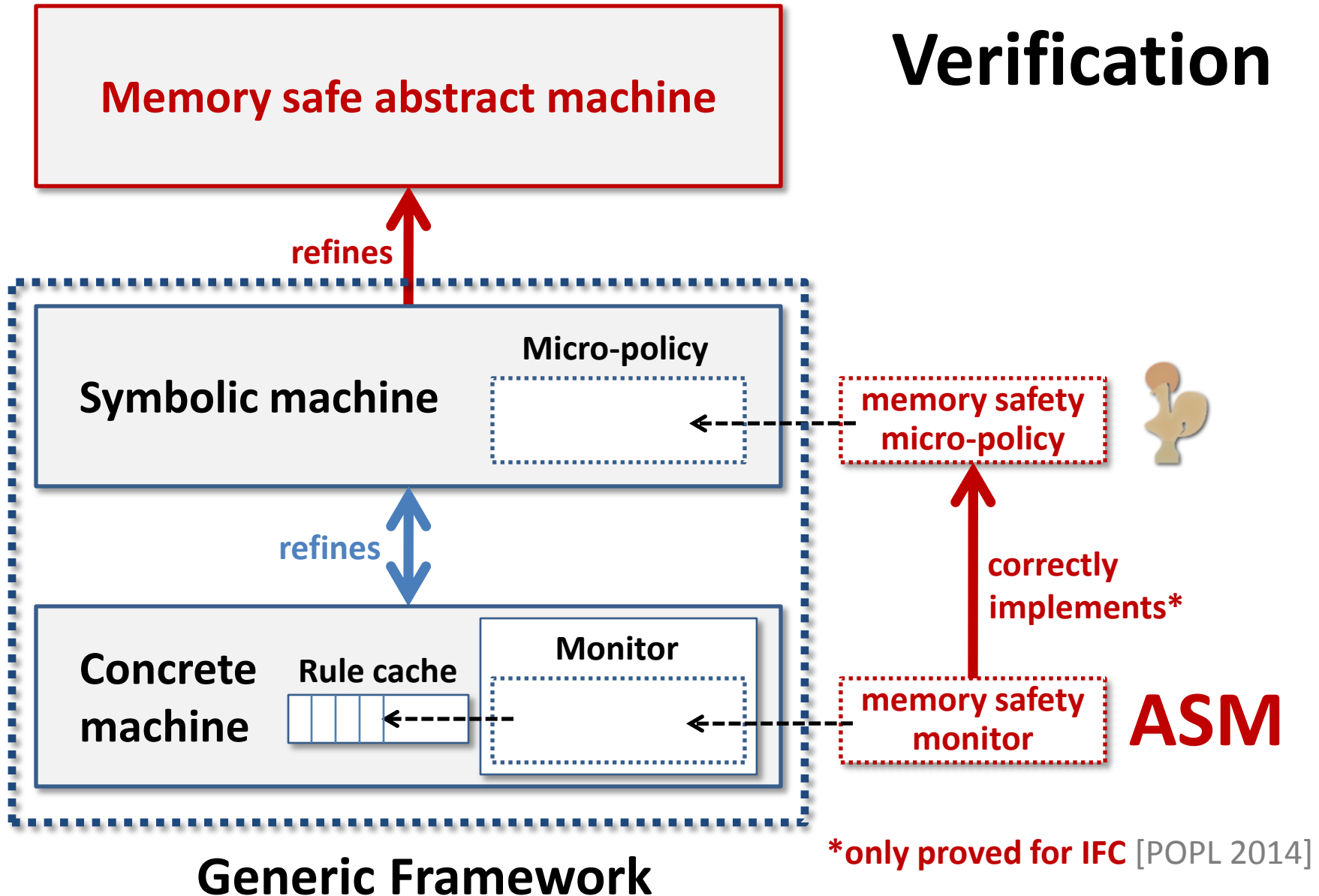
\*only proved for IFC [POPL 2014]

# Verification



\*only proved for IFC [POPL 2014]

# Verification



$$P \in \{IFC, CFI\}$$

**Abstract machine for P**

**Symbolic machine**

**Micro-policy**

**P**

**Concrete machine**

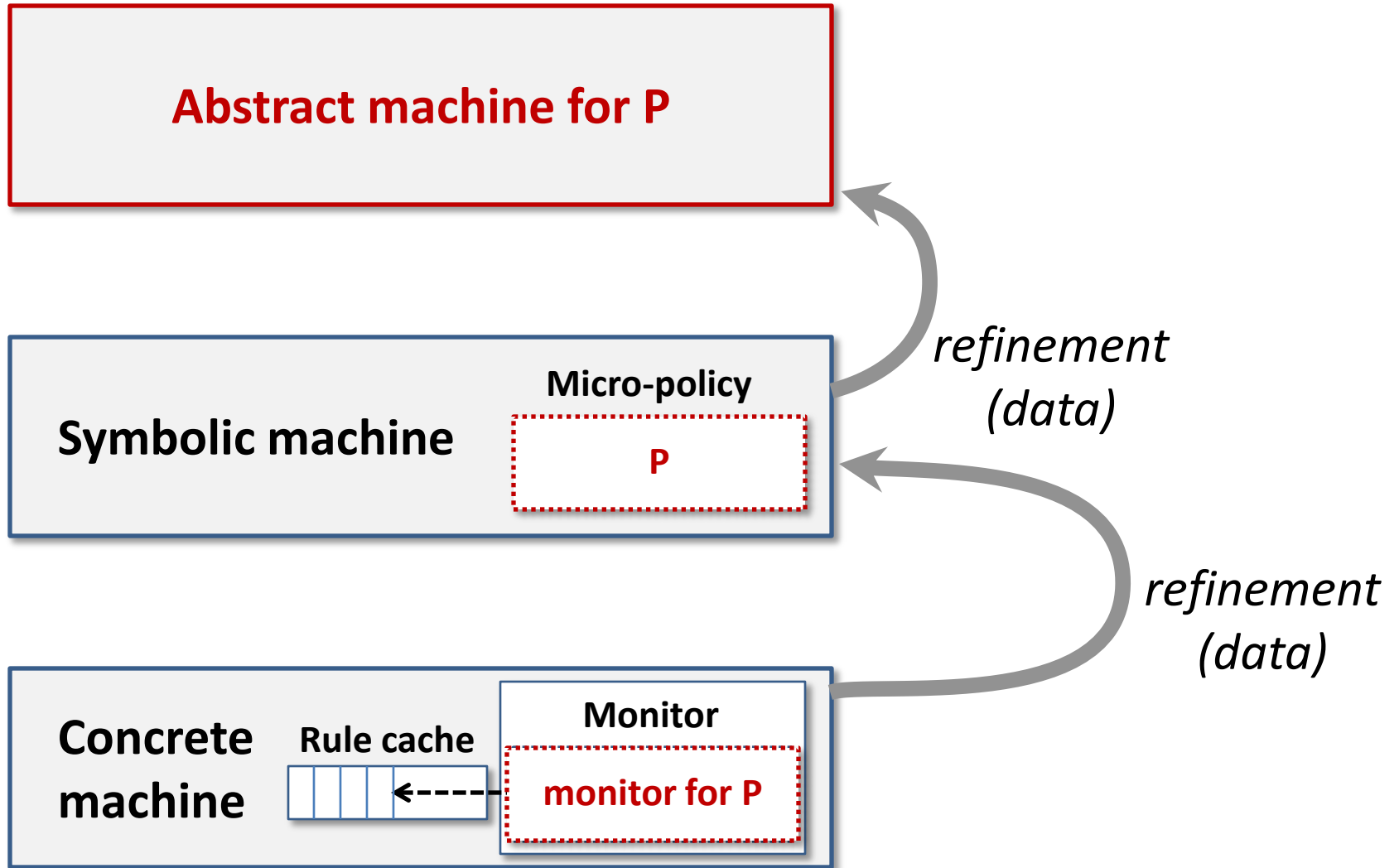
**Rule cache**



**Monitor**

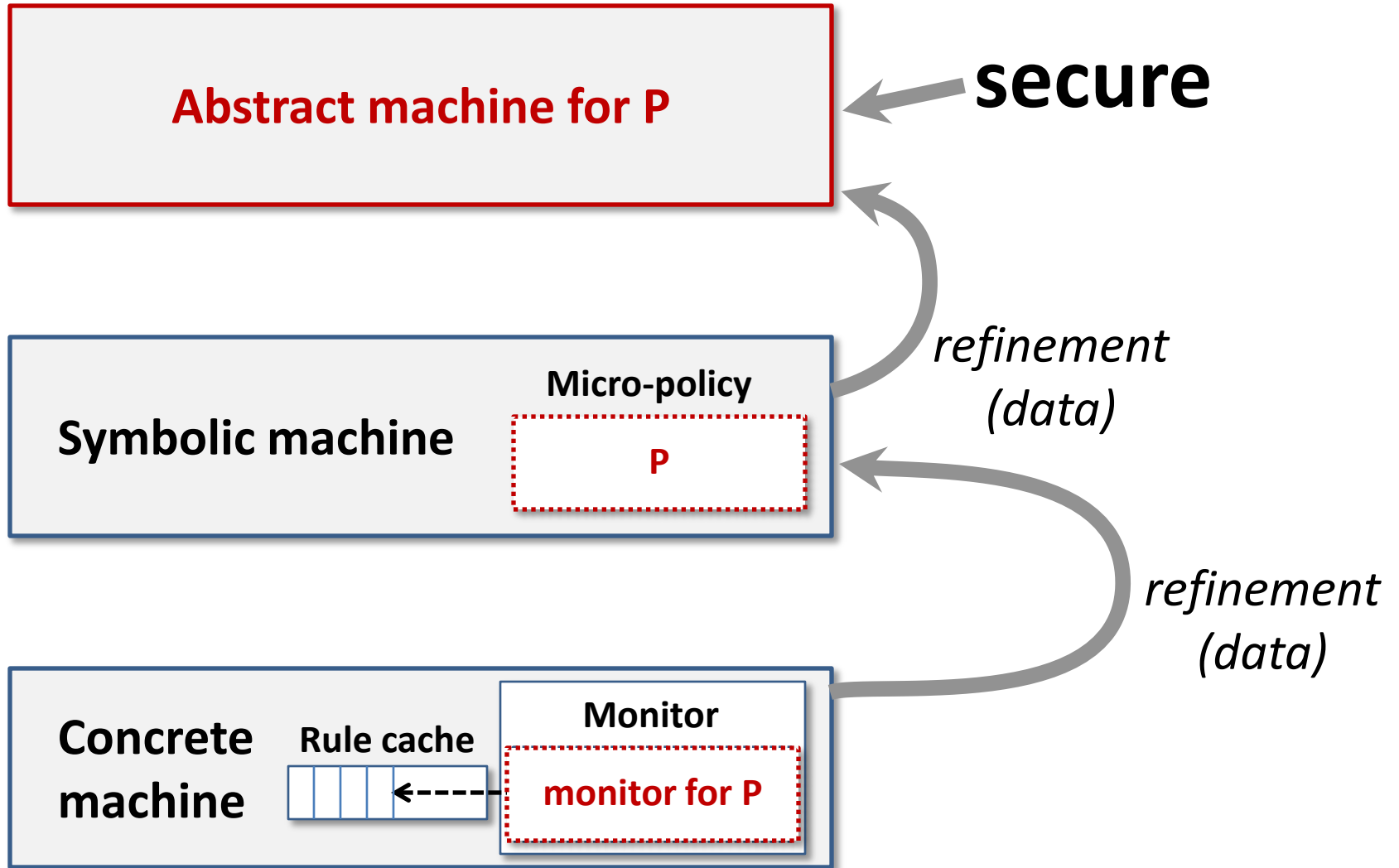
**monitor for P**

$P \in \{IFC, CFI\}$

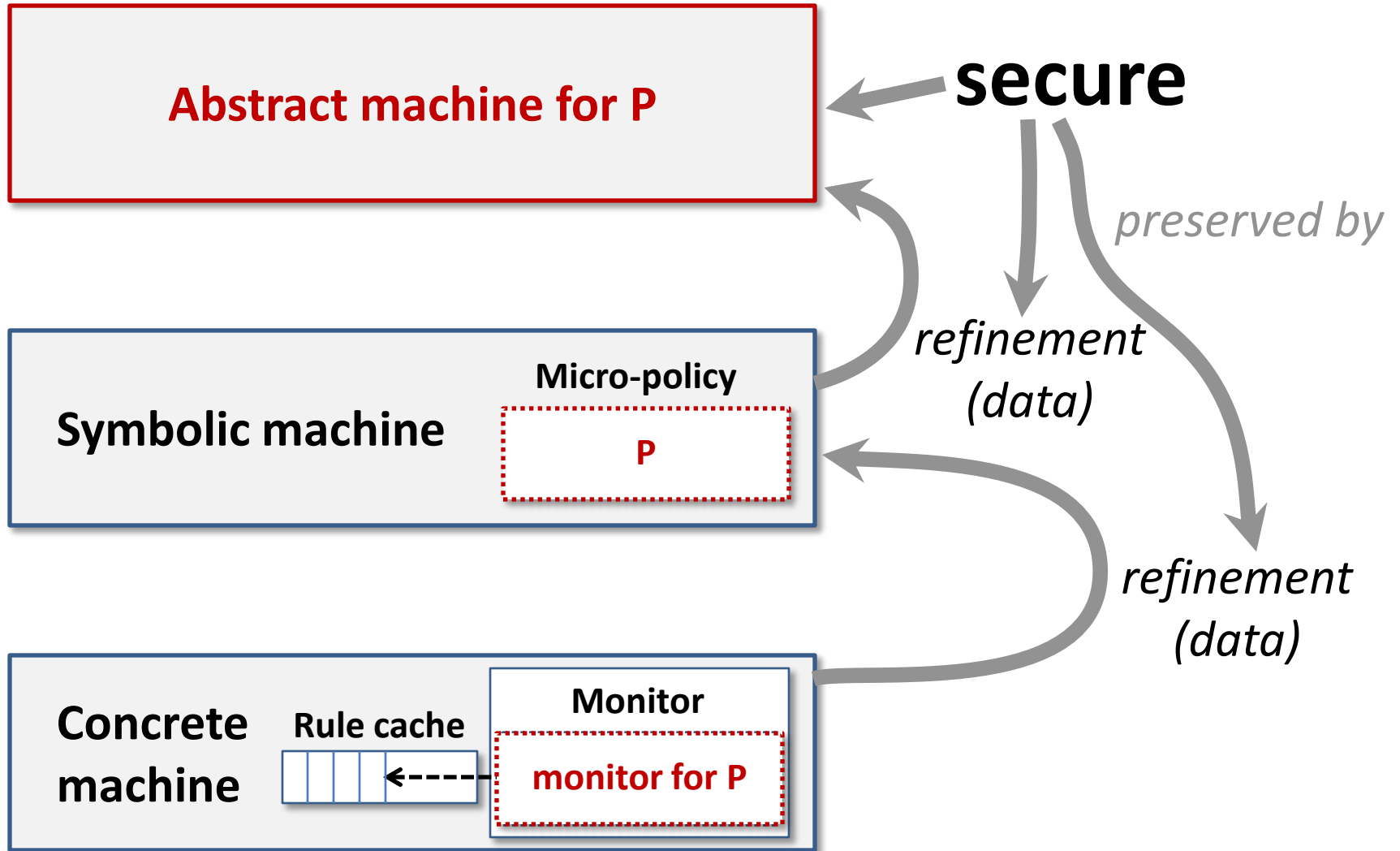




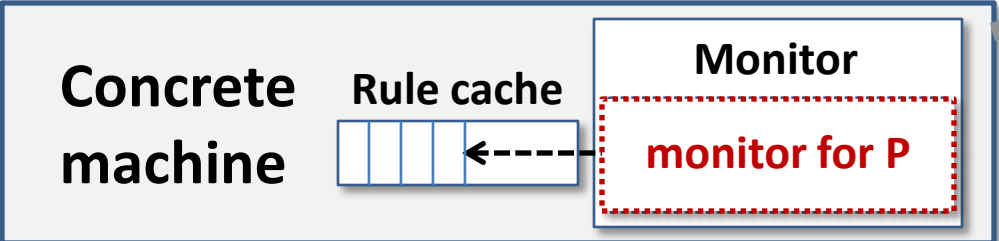
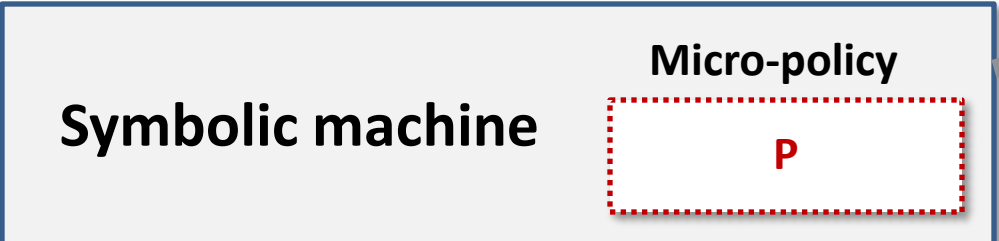
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$P \in \{IFC, CFI\}$



**secure**

*preserved by*

*refinement  
(data)*

*refinement  
(data)*

**secure**

# Future verification challenges

1. Proofs for **real RISC architecture** (e.g. ARM)
2. Verify all monitors down to **machine-code level**
3. Formally study micro-policy **composition**
4. Devise **generic meta-language** for micro-policies
5. Study **more micro-policies** (e.g. stack protection, ...)
6. Formally study **expressive power** of micro-policies
7. Interaction with **loader** and **compiler** (static + dynamic)
8. ... and **operating system** (e.g. protect the OS itself)